Exhibit 1

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Devoe et al.

(10) **Patent No.: US 6,816,356 B2**
(45) **Date of Patent: Nov. 9, 2004**

(54) **INTEGRATED BROADBAND CERAMIC CAPACITOR ARRAY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/412,992**

(22) Filed: **Apr. 14, 2003**

(65) **Prior Publication Data**

US 2004/0042156 A1 Mar. 4, 2004

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/150,202, filed on May 17, 2002, now Pat. No. 6,587,327.

(51) **Int. Cl.**[7] **H01G 9/042**; H01G 9/045; H01G 4/32

(52) **U.S. Cl.** **361/309**; 361/303; 361/311

(58) **Field of Search** 361/301.4, 303, 361/306.1, 306.3, 308.2, 309, 328–330, 310–311

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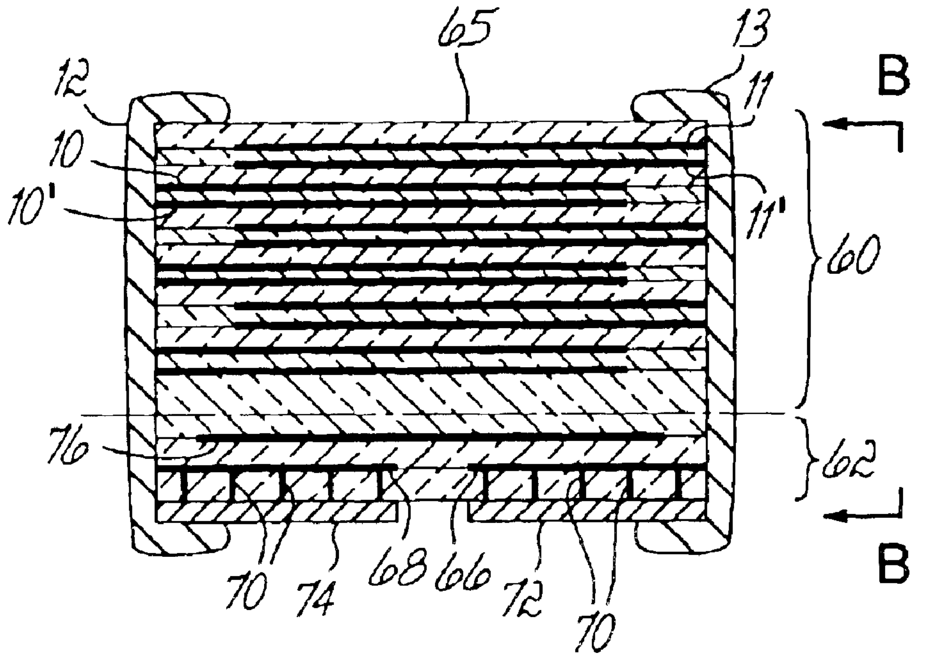
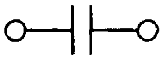
Primary Examiner—Eric Thomas
(74) *Attorney, Agent, or Firm*—Wood, Herron & Evans, L.L.P.

(57) **ABSTRACT**

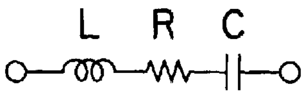
A monolithic capacitor structure includes opposed and overlapping plates within a dielectric body, which are arranged to form a lower frequency, higher value capacitor. Other conductive structure is located either inside the dielectric body or on an external surface thereof and is effective to form a higher frequency, lower value capacitor in parallel with the lower frequency, higher value capacitor. The resulting array of combined series and parallel capacitors integral with the dielectric body provides effective wideband performance in an integrated, cost-effective structure.

34 Claims, 7 Drawing Sheets

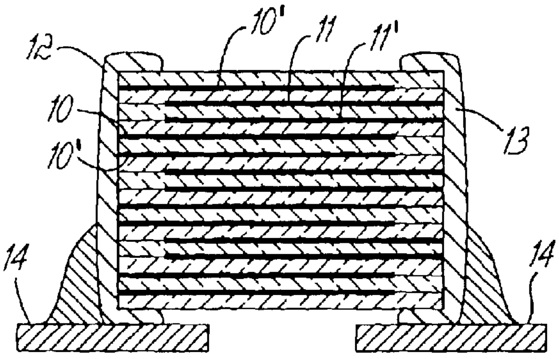




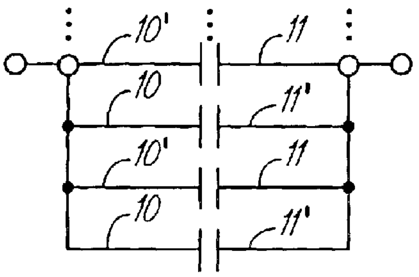
PRIOR ART
FIG. 1A



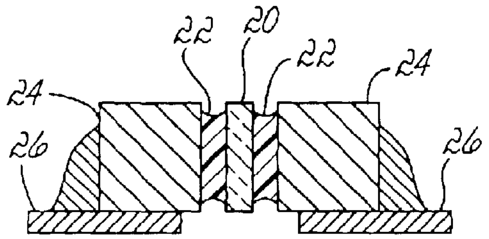
PRIOR ART
FIG. 1B


10'
11
11'
12
10
10'
13
14
14

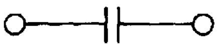
PRIOR ART
FIG. 2A


10'
11
10
11'
10'
11
10
11'

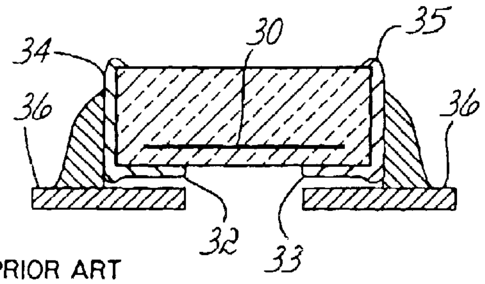
PRIOR ART
FIG. 2B


22
20
22
24
24
26
26

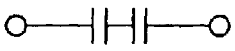
PRIOR ART
FIG. 3A



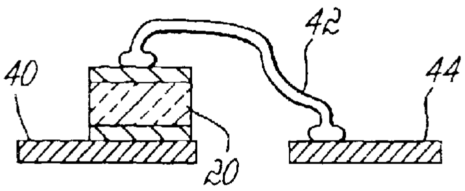
PRIOR ART
FIG. 3B


30
35
34
36
36
32
33

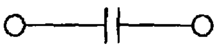
PRIOR ART
FIG. 4A



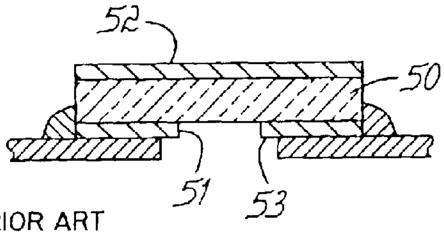
PRIOR ART
FIG. 4B



PRIOR ART
FIG. 5A



PRIOR ART
FIG. 5B

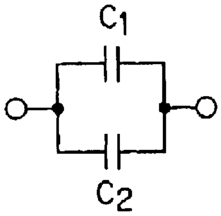


PRIOR ART

FIG. 6A

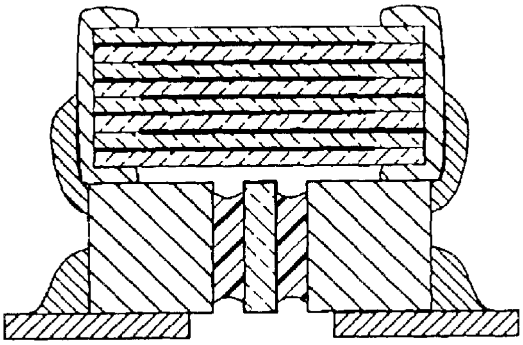
PRIOR ART

FIG. 6B



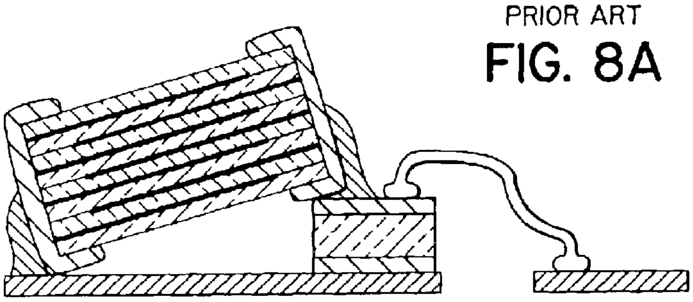
PRIOR ART

FIG. 7



PRIOR ART

FIG. 8A



PRIOR ART

FIG. 8B

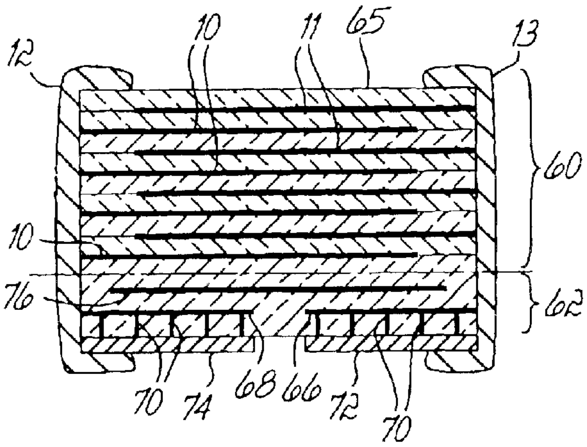

10
11
65
12
13
60
10
76
62
70
74
68
66
72
70

FIG. 9A

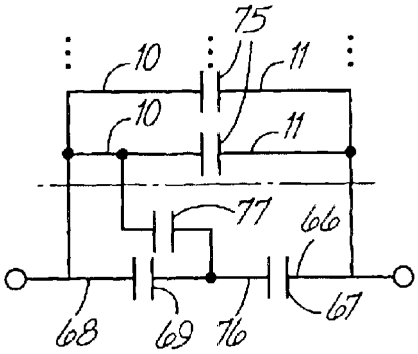

75
10
11
10
11
77
66
68
69
76
67

FIG. 9B

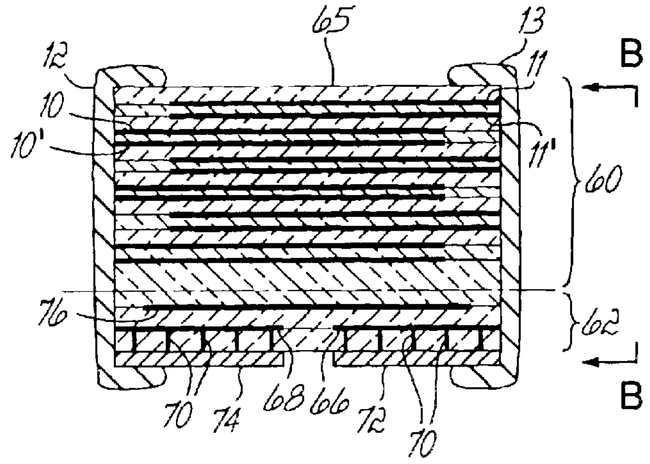

65
13
12
11
B
10
10'
11'
60
76
62
B
70 74 68 66 72 70

FIG. 10A

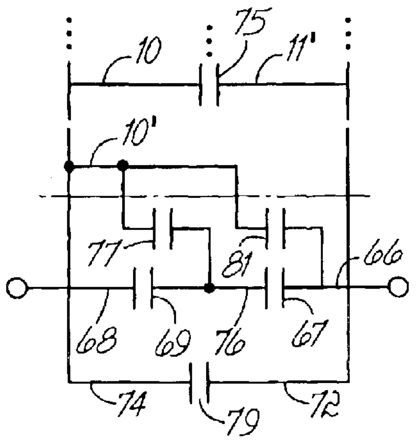

75
10
11'
10'
77
81
66
68 69 76 67
74 79 72

FIG. 10B

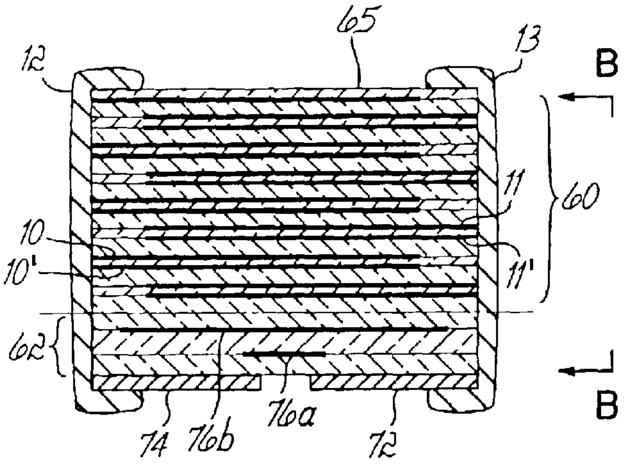

65
13
12
B
11
60
10
10'
11'
62
B
74 76b 76a 72

FIG. 11A

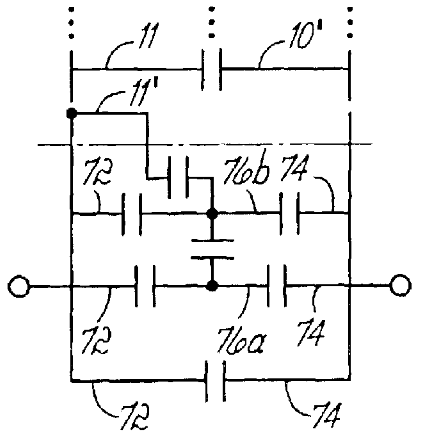

11
10'
11'
72
76b
74
72
76a
74
72
74

FIG. 11B

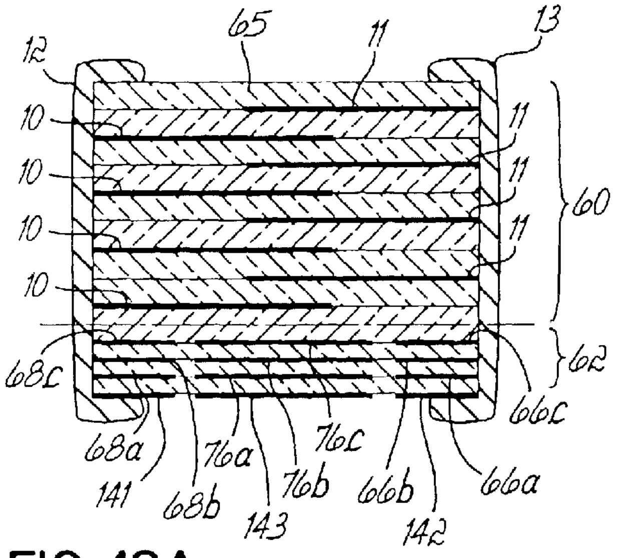

65
11
12
13
10
10
10
10
11
11
11
60
62
68c
66c
68a
141
76a
68b
143
76b
76c
66b
142
66a

FIG. 12A

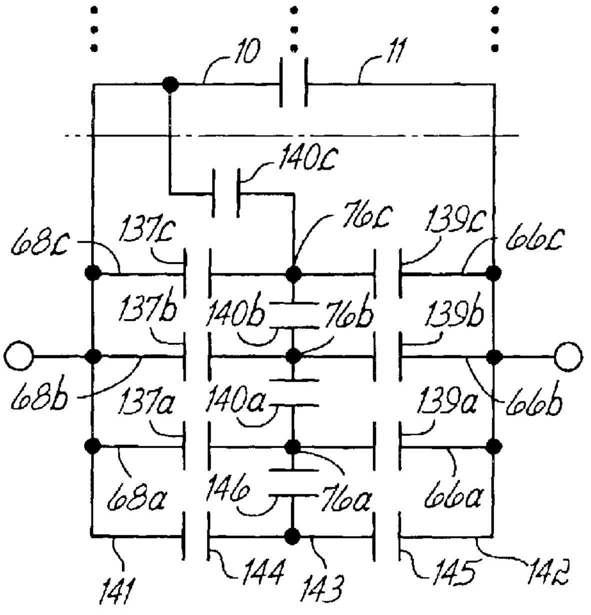

10
11
140c
68c
137c
76c
139c
66c
137b
140b
76b
139b
68b
137a
140a
139a
66b
68a
146
76a
66a
141
144
143
145
142

FIG. 12B

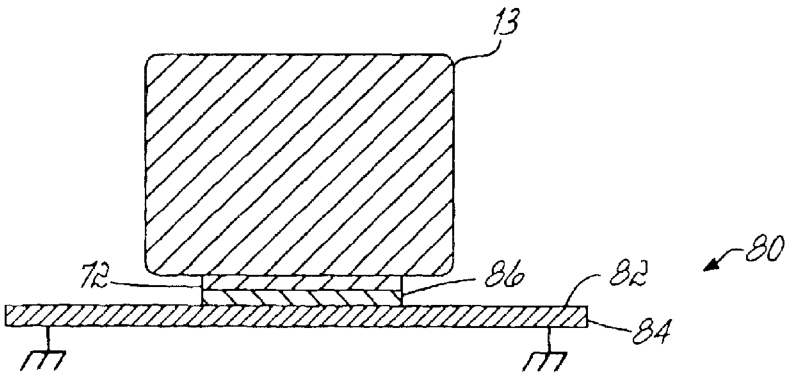
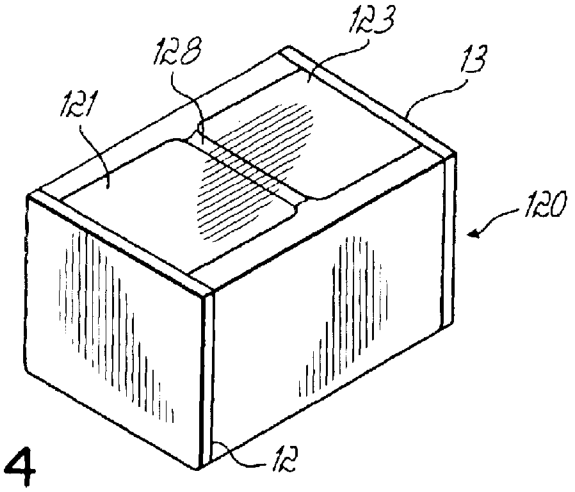
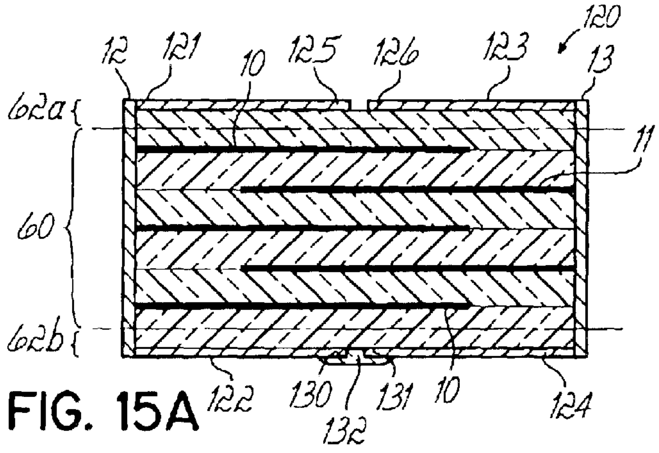

13
80
72
86
82
84

FIG. 13



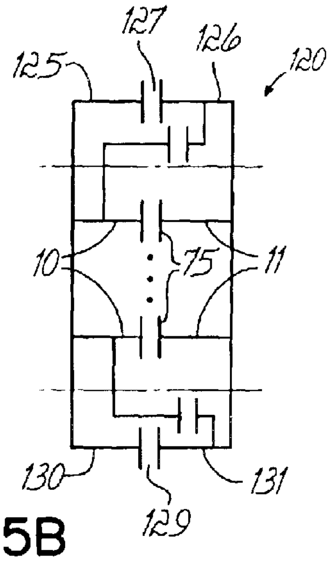
123
128
13
121
120
12

FIG. 14



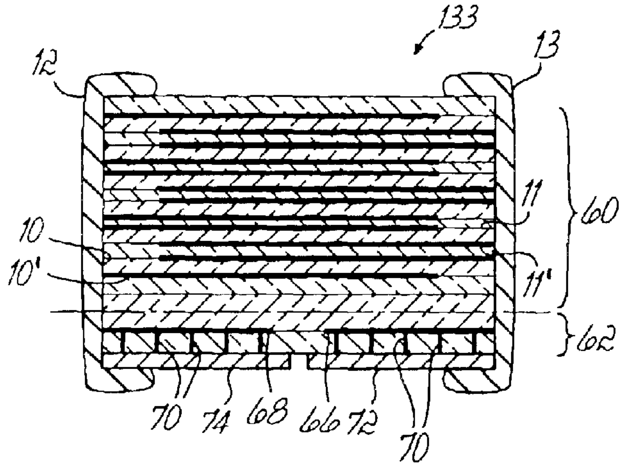
120
12
121
10
125
126
123
13
62a
11
60
62b
122
130
131
10
124
132

FIG. 15A



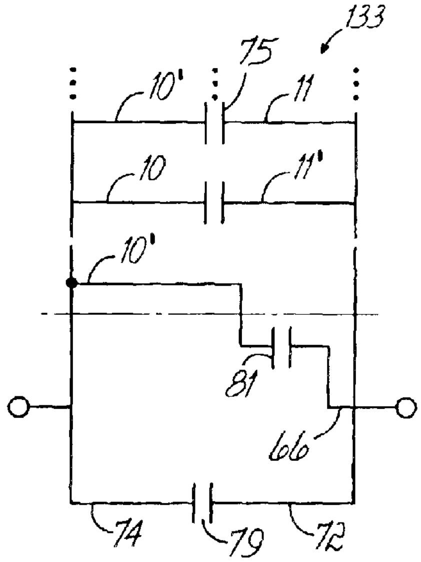
127
126
125
120
10
75
11
130
131
129

FIG. 15B



133
12
13
11
60
10
10'
11'
62
70
74
68
66
72
70

FIG. 20A



133
75
10'
11
10
11'
10'
81
66
74
79
72

FIG. 20B

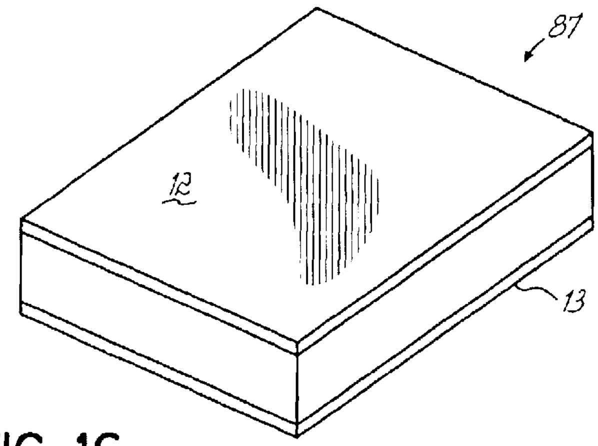


FIG. 16

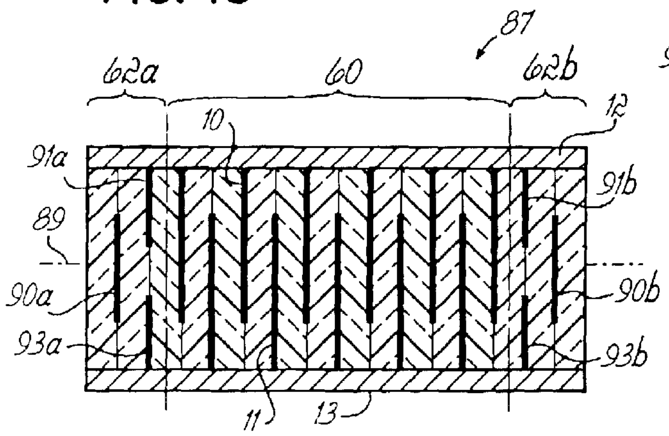

87
62a
60
62b
10
12
91a
89
90a
93a
91b
90b
93b
11
13

FIG. 17A

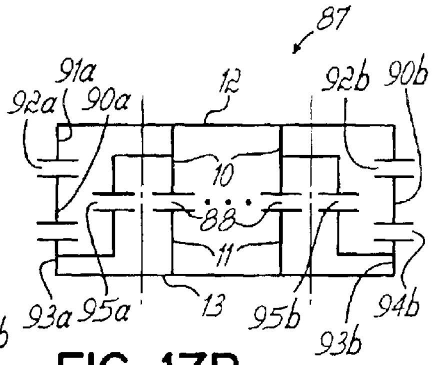

87
91a
92a
90a
12
92b
90b
10
88
11
93a
95a
13
95b
94b
93b

FIG. 17B

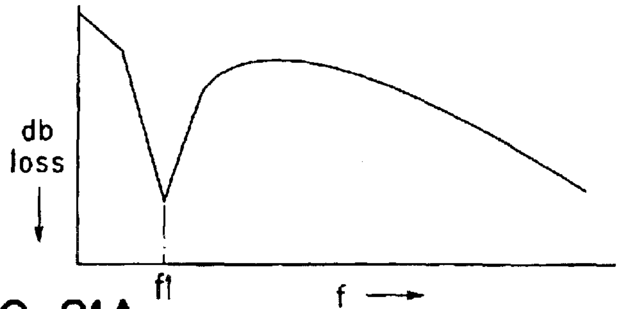


FIG. 21A

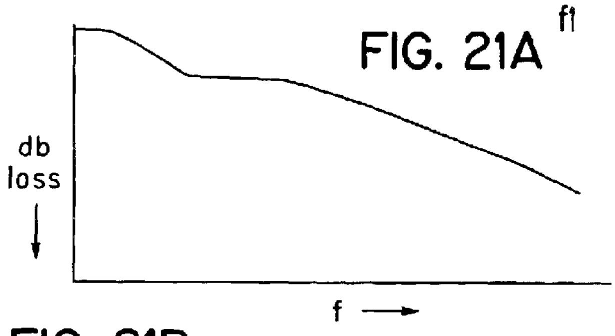
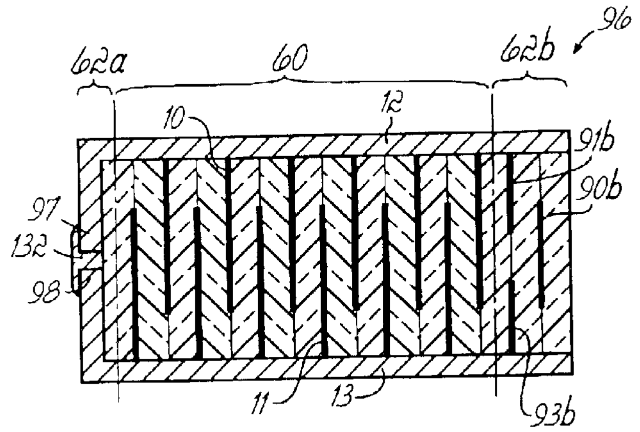
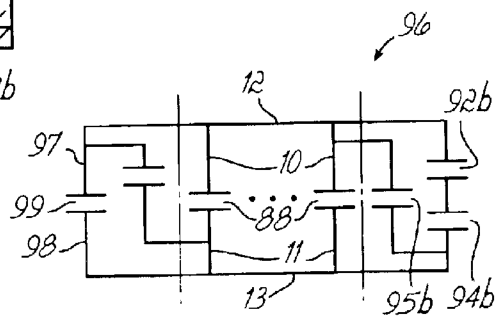


FIG. 21B



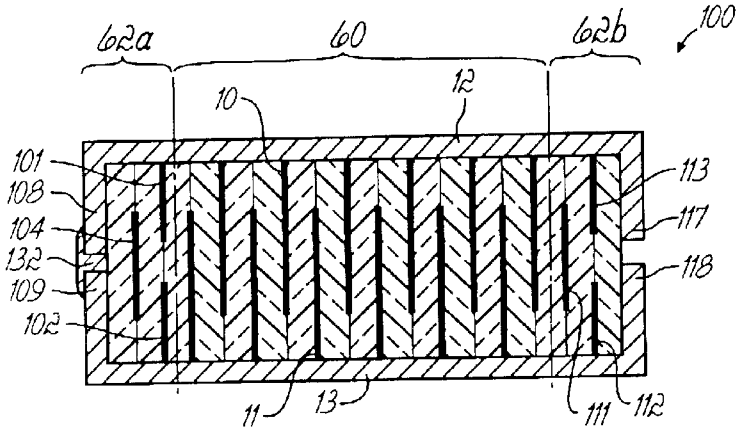
96
62a
60
62b
10
12
91b
90b
97
132
98
11
13
93b

FIG. 18A



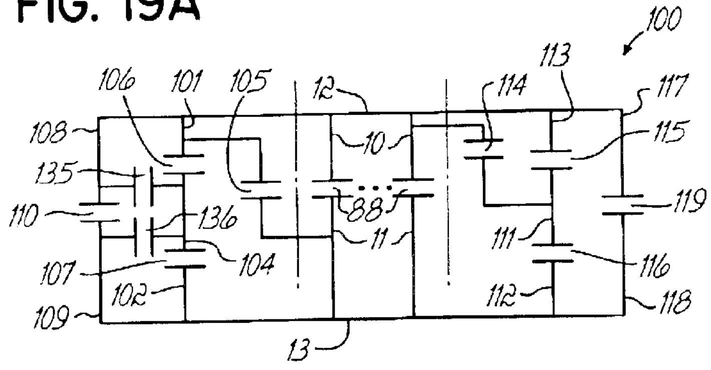
96
12
92b
97
10
99
88
98
11
13
95b
94b

FIG. 18B



100
62a
60
62b
10
12
101
108
104
132
109
102
113
117
118
11
13
111
112

FIG. 19A



100
113
106
101
105
12
114
117
108
10
115
135
88
119
110
136
11
111
104
116
107
102
112
118
109
13

FIG. 19B

INTEGRATED BROADBAND CERAMIC CAPACITOR ARRAY

This application is a continuation-in-part of U.S. application Ser. No. 10/150,202, filed May 17, 2002, now U.S. Pat. No. 6,587,327.

FIELD OF THE INVENTION

The present invention relates to miniature monolithic capacitors.

BACKGROUND OF THE INVENTION

The development of integrated circuits has made it possible to place many circuit elements in a single semiconductor chip. Where part or all of the circuit is an analog circuit, such as a radio frequency transmitter or receiver, audio amplifier, or other such circuit, circuit design requires lumped elements that cannot be readily realized in monolithic integrated circuits. Capacitors in particular are frequently created as separate elements from the integrated circuit. The electronic device thus typically includes monolithic integrated circuits combined with external capacitors.

For such applications, monolithic ceramic capacitors have been used. For example, single capacitors made of ceramic materials, are known in the art. These are relatively small in size and can be surface mounted to a surface mount circuit board, or glued and wire bonded to a substrate in a hybrid circuit layout.

FIG. **1**A shows a lumped element model for a capacitor. In this ideal model, the capacitor provides an ideal voltage/current relationship:

$$i = C\frac{dv}{dt}$$

Unfortunately, particularly at high frequencies, capacitors used in electronic circuits deviate substantially from this ideal relationship. These deviations are generally modeled as an equivalent series resistance and equivalent series inductance, along with a capacitance that varies over frequency. In accordance with this model, a capacitor behaves as a series L-R-C circuit as illustrated in

FIG. **1**B. At lower frequencies, the dominant impedance is the capacitive element C; however, at increasing frequencies the impedance of the capacitive element C decreases and the impedance of the inductive element L increases; until, at the resonant angular frequency $(LC)^{-0.5}$, the inductive element becomes predominant, and the element ceases performing as a capacitor. Simultaneously, the capacitor dissipates some stored energy (typically through heating of conducting plates and traces), as represented by the series resistance R.

Capacitor design typically must compromise between capacitance value and equivalent series resistance and inductance; greater capacitance typically can be created only at the cost of increased series resistance and inductance. Accordingly, equivalent series resistance and inductance are not avoidable, and electronic design must take them into account, particularly in high frequency products such as broadband receiver/transmitters, short wave devices, and the like.

Various monolithic ceramic structures have been developed to provide relatively small capacitors for highly integrated applications. A first such structure, shown in FIG. **2**A, is known as a “multilayer ceramic capacitor”. This structure is formed by stacking sheets of green tape or greenware, i.e., thin layers of a powdered ceramic dielectric material held together by a binder that is typically organic. Such sheets, typically, although not necessarily, of the order of five inches by five inches, can be stacked with additional layers, thirty to one hundred or so layers thick. After each layer is stacked, conductive structures are printed on top of the layer, to form internal plates that form the desired capacitance. When all layers are stacked, they are compressed and diced into capacitors. Then, the compressed individual devices are heated in a kiln according to a desired time-temperature profile, driving off the organic binder and sintering or fusing the powdered ceramic material into a monolithic structure. The device is then dipped in conductive material to form end terminations for the internal conductive structures, suitable for soldering to a surface mount circuit board or gluing and wire bonding to a hybrid circuit.

The printed conductive structures are arranged in a pattern that provides one or more parallel-plate capacitors. For example, in the typical structure shown in FIG. **2**A, internal plates **10** and **11** have been formed which extend from alternate sides of the combined structure. The conductive material **12** and **13** at each end forms a common connection point for each plate extending to that side. Plates **10** extend in pairs, each including an upper plate **10** and a lower plate **10**' from the left side, and plates **11** extend similarly in pairs, each including an upper plate **11** and a lower plate **11**' from the right side, forming parallel plate capacitors between each set of adjacent plates **10** and **11**' and **10**' and **11**. The illustrated structure is arranged to reduce equivalent series resistance and inductance, by virtue of the plates **10** and **11** extending in pairs from each side. In other embodiments, plates extend individually from opposite sides, such as in the multilayer ceramic capacitor shown in FIGS. **7**A and **7**B and discussed below.

Each pair of overlapping plates **10** and **11** extending from opposite side metallizations **12** and **13**, forms a parallel plate capacitor, such that the entire device forms a network of parallel connected capacitors as shown in FIG. **2**B, which can be soldered to the traces **14** of a surface mount circuit board. The resulting equivalent capacitance value is relatively large for the device size, albeit subject to imperfections due to resistance in the many current-carrying conductive structures, and inductance resulting from many plates carrying currents flowing in opposite directions.

FIG. **3**A shows an alternative known capacitor structure developed by Dielectric Laboratories, Inc. of Cazenovia, N.Y. and described in detail in U.S. Pat. No. 6,208,501. This structure includes a ceramic chip **20** having conductive end plates on its opposed surfaces, which is bonded by conductive epoxy **22** to conductive end terminations **24** which can then be soldered to the traces **26** on a surface mounting circuit board. As can be seen in FIG. **3**B, the net effect is a single capacitor, rather than a parallel array, between the conductive ends of the device. As there is only one capacitor in this device, it has good high frequency performance (reduced resistance and inductance) but has a relatively low capacitance value.

FIG. **4**A shows a second alternative capacitor structure developed by American Technical Ceramics Corporation and described in detail in U.S. Pat. No. 5,576,926. This structure includes a layered ceramic chip having an internal conductive plate **30** positioned to overlay conductive plates **32** and **33** extending along an outer surface of the device from conductive end terminations **34** and **35**. As before, the conductive end terminations may be readily soldered to the traces **36** of a surface mount circuit board. As seen in FIG. **4**B, the net effect is a series combination of two capacitors, between the conductive ends of the device. As in this case there is a series combination of capacitors (which has a lower capacitance value than either capacitor individually), the device has good high frequency performance but relatively low capacitance value.

A third alternative capacitor is shown in FIG. 5A. Here, the ceramic chip **20** with opposed conductive surfaces, shown in FIG. 3A, has been mounted directly to the trace **40** of a hybrid circuit device. The opposed side of the capacitor has been wire bonded through wire bond **42**, to the opposite trace **44** of the hybrid device. In this case, the equivalent circuit diagram (FIG. 5B), and performance issues are the same as those with regard to the capacitor of FIG. 3A.

A final alternative capacitor is shown in FIG. 6A. Here, a series capacitor (FIG. 6B) has been formed between metallizations **51**, **52** and **53** that are strictly on the outer surfaces of a ceramic chip **50**. This alternative is similar to the device shown in FIG. 4A, but the internal metallization has been moved to the outer surface. This device is less complex to manufacture than the device of FIG. 4A, but provides lower capacitance value owing to the distance between the metallization layers **51** and **53** and the opposed metallization layer **52**.

As can be seen, each known structure represents a tradeoff between capacitance value and broadband performance. One known approach to managing series resistance and series inductance, is to parallel connect two capacitors, such as shown in FIG. **7**. In FIG. **7**, a larger value capacitor C**1**, chosen for its large capacitance value, is connected in parallel to a smaller value capacitor, chosen for its small equivalent series resistance. As will be appreciated, this circuit exhibits multiple resonant frequencies, a first at the frequency $(L1C1)^{-0.5}$, and a second at the frequency $(L2C2)^{0.5}$. Typically the larger valued capacitor C**1** would have the larger series resistance and inductance value and thus the lower resonant frequency, whereas the smaller valued capacitor C**2** would be chosen for high frequency performance resulting from low series resistance and series inductance values. At low frequencies, the larger value of C**1** will produce acceptable performance, whereas at higher frequencies, where C**1** behaves increasing less like a capacitor and more like an inductance, C**2** will be below its resonant frequency and perform well as a capacitor throughout the frequency of interest.

The parallel capacitor approach has been utilized in conjunction with ceramic chip capacitors, to improve the high frequency performance of those capacitors. Specifically, referring to FIG. **8**A, one known approach to forming a broadband ceramic capacitor structure, uses a multilayer capacitor such as that described above with reference to FIG. **2**A, stacked above and soldered or bonded to a single layer, high frequency capacitor such as that described above with reference to FIG. **3**A. The resulting combined structure is wave soldered or bonded together with epoxy, producing a parallel combination of low and high-frequency capacitors seeking to achieve broadband performance. A second known implementation of this concept is shown in FIG. **8**B. There, one of the side terminals of a multilayer capacitor such as described above with reference to FIG. **2**A, is tilted against the upper surface of a single-layer, high frequency capacitor such as that described above with reference to FIG. **6**A. The upper surface of the single-layer capacitor thus forms a first terminal of a parallel capacitor combination, that is wire bonded to a circuit board trace **36** in the manner described above with reference to FIG. **5**A. The opposite side terminal of the multi-layer capacitor and the bottom surface of the single-layer capacitor are connected to a second trace **36** of the circuit board, thus forming the second terminal of the combined parallel capacitor combination.

While parallel capacitor combinations such as shown in FIGS. **8**A and **8**B have been used with some success in commercial devices, these combinations suffer from a number of drawbacks. First, the measured capacitance of these parallel combinations exhibit variations (resonances and dropouts), likely due to a mismatch between the resonances of the effective L-R-C circuits that are created by the parallel connected capacitors. Furthermore, the upper frequency response of even these parallel combinations may not meet the requirements of very wide band (GHz) devices in current use. Also, the mechanical stacking of dual ceramic capacitors in the manner shown is not easily compatible with "tape and reel" assembly methods and thus, are cumbersome and expensive to implement in mass production. Further, mechanically stacking dual ceramic capacitors increases the overall height of the circuit board assembly above that of a board having only single ceramic capacitors.

There accordingly is a remaining need for a broadband capacitor meeting the performance needs of modern wideband circuits, while maintaining the size and cost efficiencies of existing ceramic capacitors.

SUMMARY OF THE INVENTION

The present invention provides a capacitor having an effective wideband performance in an integrated, cost-effective structure. The capacitor of the present invention is an integrated array of capacitors connected in series and/or parallel circuits in a substantially monolithic dielectric body. The composition of the integrated capacitor array can be varied in order to tune the wideband capacitor to a particular application. Further, the integrated capacitor array of the present invention provides superior performance by providing less insertion loss than combinations of discrete capacitors. In addition, the wideband capacitor of the present invention is smaller and easier to handle and mount on a circuit board than combinations of discrete capacitors.

In accordance with principles of the present invention, a monolithic capacitor includes both a multi-layer, lower frequency, higher valued capacitor and a higher frequency, lower valued capacitor. More specifically, a dielectric body includes a series of conductive plates arranged in a substantially parallel and opposed configuration in one region of the body, to form the lower frequency, lower value, capacitor. In another region of the dielectric body, other conductive structures or plates are positioned to form a higher frequency, lower value capacitance in parallel with the lower frequency, higher value capacitance.

In specific disclosed embodiments, the conductive structures may be one or more conductive plates positioned inside the dielectric body with respect to a conductive floating plate. Alternatively, the conductive structures may be placed either on an external surface of the dielectric body, or inside the dielectric body and connected by one or more vias to plates on an external surface of the dielectric body. The conductive structures can further be opposed edges that are positioned to form a fringe-effect capacitance.

In the disclosed embodiments, the capacitor has a substantially monolithic dielectric body formed from a plurality of ceramic tape layers laminated together in a green ceramic state and fired to form a sintered or fused monolithic ceramic structure. However, other dielectric materials and assembly methods may be used. Further, in the disclosed embodiments the dielectric body has a hexahedral shape, with electrical contacts positioned on opposed end surfaces. However, other shapes may also be used.

These embodiments, and the above and other objects and advantages of the present invention shall be made apparent from the accompanying drawings and the description thereof.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with a general description of the invention given above, and the detailed description of the embodiments given below, serve to explain the principles of the invention.

FIGS. **1**A and **1**B illustrate a capacitor and the known equivalent model therefor.

FIGS. **2**A and **2**B illustrate a known multilayer monolithic capacitor structure and its equivalent circuit diagram.

FIGS. **3**A and **3**B illustrate a known high frequency single layer monolithic capacitor structure and its equivalent circuit diagram.

FIGS. **4**A and **4**B illustrate a known high frequency buried layer monolithic capacitor structure and its equivalent circuit diagram.

FIGS. **5**A and **5**B illustrate a known high frequency single layer monolithic capacitor structure and its equivalent circuit diagram.

FIGS. **6**A and **6**B illustrate a known high frequency single layer monolithic capacitor structure and its equivalent circuit diagram.

FIG. **7** illustrates a circuit diagram of a known parallel combination of capacitors to form a wideband capacitor.

FIGS. **8**A and **8**B illustrate known implementations of a parallel combination of capacitors using known capacitors previously illustrated.

FIG. **9**A illustrates a first embodiment of an integrated wideband capacitor in accordance with one aspect of the present invention, and FIG. **9**B illustrates an equivalent circuit diagram.

FIG. **10**A illustrates a second embodiment of an integrated wideband capacitor in accordance with further aspects of the present invention, and FIG. **10**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **11**A illustrates a third embodiment of an integrated wideband capacitor in accordance with further aspects of the present invention, and FIG. **11**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **12**A illustrates a fourth embodiment of an integrated wideband capacitor in accordance with further aspects of the present invention, and FIG. **12**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **13** is an end view of the embodiments of FIGS. **10**A and **11**A in accordance with further aspects of the present invention.

FIG. **14** is a perspective view of another embodiment of an integrated wideband capacitor in accordance with the principles of the present invention.

FIG. **15**A illustrates an embodiment of the capacitor of FIG. **14**, and FIG. **15**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **16** is a perspective view of a still further embodiment of an integrated wideband capacitor in accordance with the principles of the present invention.

FIG. **17**A illustrates an embodiment of the capacitor of FIG. **16**, and FIG. **17**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **18**A illustrates another embodiment of the capacitor of FIG. **16**, and FIG. **18**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **19**A illustrates a further embodiment of the capacitor of FIG. **16**, and FIG. **19**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **20**A illustrates a still further embodiment of the capacitor of FIG. **16**, and FIG. **20**B illustrates an equivalent circuit diagram for this embodiment.

FIG. **21**A is a graph representing insertion loss of a combination of discrete capacitors such as those shown in FIG. **8**A.

FIG. **21**B is a graph representing insertion loss of an integrated wideband capacitor such as that shown in FIG. **9**A.

DETAILED DESCRIPTION

Referring now to FIG. **9**A, a first embodiment of an integrated capacitor in accordance with certain aspects of the invention, can be described. In this embodiment, an integrated multi-layer and high frequency capacitor includes an upper section **60** including a multi-layer structure similar to that discussed above with reference to FIG. **2**A, including plates **10** and **11** extending from conductive contacts **12** and **13**, respectively, on opposite sides of a ceramic dielectric body. In this embodiment, individual plates extend from each side contact, rather than pairs of plates as shown in FIG. **2**A. Using single plates in this manner increases the series inductance and resistance, for the reason that more current is caused to flow over each individual plate; however, more plates can be included in the capacitor using single plates, allowing an increase in capacitance value. Thus, the decision to use single or multiple plates is a tradeoff between capacitance and series resistance and inductance.

In the embodiment of FIG. **9**A, a high frequency capacitor is formed in a lower section **62**, from two additional internal plates **66** and **68** which extend from the end contacts **13** and **12**, respectively. These internal plates are connected by vias **70** to external conductive plates **72** and **74**, respectively, which are printed on the exterior of the ceramic dielectric body **65**. Multiple conductive paths are thus provided to the interior plates **66** and **68** to reduce series resistance. Plates **66** and **68** are capacitively coupled to a floating interior plate **76**, forming a series combination of capacitances **67**, **69**, from plate **66** to plate **76**, and from plate **76** to plate **68**.

It has been found that the high frequency performance of the device of FIG. **9**A is affected by the relative position of plate **76** and the nearest multi-layer plate **10** in upper section **60** of the device directly above plate **76**. Accordingly, the high frequency performance is a function of the capacitance between plate **76** and the plate **10** immediately above plate **76** in the upper section **60** of the device.

Referring to FIG. **9**B, the equivalent circuit diagram of operative capacitances in the device of FIG. **9**A, includes not only capacitances **67**, **69**, **75** between plates **66**, **76** and **68**, and between plates **10** and **11**, respectively, but further capacitances **77** between plate **76** and plate **10** from the upper section. The multiplicity of capacitances and their interrelationship is believed to permit fine-tuning of high frequency response of the device, e.g. by tuning out resonances that cause dips in the curve of capacitance vs. frequency. When the multiple capacitors have peak performance areas that are closely spaced in the high frequency (GHz) range of operation, when combined, the result can be a flatter frequency response than is possible in prior approaches of stacking multiple discrete ceramic capacitors such as shown in FIGS. **8**A and **8**B.

FIG. **21**A illustrates a typical plot of insertion loss as a function of frequency that is obtained when discreet capacitors are connected in parallel substantially as shown in FIG. **8**A. Typically, the insertion loss experiences one or more increases, such as that shown at a frequency f1. FIG. **21**B illustrates a plot of insertion loss as a function of frequency for the broadband capacitor illustrated in FIG. **9**A. As can be seen, the insertion loss is relatively smooth throughout a broad range of frequencies. In the example of FIG. **9**A, the bulk capacitance in the larger value, low frequency upper section **60** can be made to have a capacitance in a range of about 10–100 nanofarads. Further, if the capacitance in the lower value, high frequency lower section **62** is made to have a capacitance of about 82 picofarads, the insertion loss plot of FIG. **21**B is relatively smooth over a frequency range of about 10 KHz to 10 Ghz and higher.

FIG. **10**A illustrates an alternative device structure that embellishes the capacitor network described in the theory of operation of the device of FIG. **9**A. Specifically, in this device, the external conductive plates **72** and **74** in the lower section **62** of the device have been extended toward each other so as to create a capacitance between plates **72** and **74** based upon fringe electric field extending to and from the adjacent edges of those plates.

Also, the edges of floating internal plate **76** have been withdrawn toward the interior of the device, which has the effect of lowering the capacitance and inductance between plate **76** and plates **72** and **74**. The reduced capacitance results from the reduced area of plate **76** that is opposed by plates **72** and **74**. The reduced inductance results from reduced distances through which there are opposed current flows in plates **76**, **72** and **74**. Furthermore, the withdrawal of the plate **76**, permits some direct capacitive coupling between plate **66** of the lower section **62** of the device and plate **10**' of the upper section of the device, introducing an additional capacitance to the device.

Finally, in this device, dual plates have been used in the upper section **60** of the device to reduce series resistance and inductance, albeit at some expense of capacitance value. The use of dual or single plates in the upper section **60** is a possible design choice for any embodiment of the invention described herein, regardless of the elements used in the lower section **62**.

Thus, the equivalent circuit diagram of the device of FIG. **10**A, shown in FIG. **10**B, as compared to the diagram of FIG. **9**B, includes an additional capacitance **79** between plates **72** and **74**. This additional capacitance is shown in dotted outline in FIG. **10**A, reflecting that the fringe capacitance between plates **72** and **74** may be relatively small compared to the other parallel plate capacitances in the remainder of the lower section **62** of the device. However, this capacitance may well affect the very high frequency performance of the device.

The equivalent circuit diagram of FIG. **10**B is further different from FIG. **9**B, in an additional capacitance **81** between plate **66** and plate **10**'. This additional capacitance will provide an additional resonance that can aid in flattening the high frequency performance of the device.

The equivalent circuit diagram of FIG. **10**B is still further different from FIG. **9**B, in that the capacitances from plates **66** and **76** to plate **10**' in the upper section **60** of the device are independently connected to the end terminal, i.e., current flows to and from plate **10**' independently of any current flow in the plates **10** and **11**' which form the lowermost parallel plate capacitor in section **60** of the device. Providing an independent current flow path, via plate **10**', for capacitive current flowing from plate **76**, may affect the equivalent series resistance and inductance of the high frequency portion of the device and thus prove an important design feature. It will be appreciated that an independent current path for capacitances coupled from the lower section **62** of the device, provided by a plate positioned in the manner of plate **10**' in FIG. **10**A, may be used in any embodiment of the invention, regardless of whether that embodiment also includes dual plates throughout the upper section **60** of the device as is the case in FIG. **10**A.

Referring now to FIG. **11**A, in a further embodiment of the invention, the upper section **60** is formed as in FIG. **10**A, of plates that extend in pairs **10**/**10**' and **11**/**11**' from the end terminals **12** and **13**. The lower section **62** includes a structure distinct from that of FIG. **10**A in several respects. First, the internal plates **66** and **68** and the vias connecting those plates to external plates **72** and **74**, have been eliminated. In the space occupied by plates **66**, **68** and **76** in the device of FIG. **10**A, are two floating plates **76**A and **76**B, which capacitively couple directly to the external plates **72** and **74**. Plate **76**A is placed closest to plates **72** and **74** and has a smaller horizontal extent than plate **76**B. Capacitive coupling can thus occur, between plates **72** and **74** and plate **76**A, as well as between plates **72** and **74** and plate **76**B. Furthermore, plates **76**A and **76**B are capacitively coupled to each other. Also, plate **76**B is capacitively coupled to the lowermost plate **11**' of the upper section **60** of the device.

The resulting complex network of capacitances is shown in FIG. **11**B. As can be seen, the network of capacitances provides a substantial number of capacitances that can be adjusted (e.g., by altering the size, placement or number of the floating plates **76**, and the size of the plates **72** and **74**), to optimize high frequency performance of the device.

Another embodiment is illustrated in FIG. **12**A. In this embodiment, single plates **10** and **11** are used in the upper section of the device. However, the single plates **10** and **11** are withdrawn relative to their positions in the devices of FIGS. **9**A, **10**A and **11**A, reducing the overlap of adjacent plates **10** and **11**. As a result, the capacitance and series inductance of the capacitors in the upper section **60** of the device are reduced, due to decreased opposed area and decreased opposed current flows. Furthermore, in the lower section **62** of the device, the arrangement of plates shown in the preceding figures has been replaced with a plurality of interior plates **66**A, **66**B and **66**C extending from terminal **13**, and a plurality of interior plates **68**A, **68**B and **68**C extending from terminal **12**, each respectively opposed edge-to-edge by one of a plurality of interior floating plate **76**A, **76**B and **76**C to form series capacitor pairs. Furthermore, the floating plates **76**A, **76**B and **76**C are capacitively coupled to each other, and the uppermost floating plate **76**C is capacitively coupled to the lowermost plate **10** of the upper section **60** of the device. The number of floating plates **76** and interior plates **66** and **68** is subject to adjustment to achieve a desired capacitance. Furthermore, the plates **66** and **68** may be positioned on alternating layers relative to plates **76** to decrease the likelihood of breakdown paths forming along layer boundaries in the ceramic dielectric material.

FIG. **12**B illustrates the equivalent circuit diagram for the device of FIG. **12**A. Notably, the plural series capacitor pairs **137**, **139** interconnected by capacitors **140** in this embodiment provide, as before, a large number of capacitances that may be adjusted to optimize high frequency performance. It will be noted that additional, variable capacitances may be created by staggering the widths of the floating plates **76** relative to the plates **66** and **68** so that plates **76**, **66** and **68** couple face-to-face to each other as well as through fringe fields coupled to the edges of those plates.

In a still further embodiment, external conductive plates **141** and **142** are connected to the external conductive contacts **12**, **13**, respectively. An external floating conductive plate **143** is placed between the ends of the conductive plates **141**, **142** and is not connected to either of the contacts **12**, **13**. As shown in FIG. **12**B, the floating conductive plate **143** is sufficiently close to the ends of the plates **141**, **142** as to form serial fringe-effect capacitances **144**, **145** therebetween and an interconnecting capacitance **146** with plate **76***a*. Again, the capacitances can be adjusted to optimize high frequency performance.

Referring now to FIG. **13**, an end view of the devices of FIGS. **10**A and **11**A can be used to discuss additional high frequency optimization steps. FIG. **13** shows a device mounted to a surface mount circuit board **80**, having a non-conductive outer surface **82** and a buried ground plane **84** of conductive material. Conductive traces **86** run along the upper surface **82** of board **80**, to interconnect components such as integrated circuits, discrete capacitors, and the like. The devices of FIGS. **10**A and **11**A include external conductive plates **74** and **76** which may be directly mounted to these conductive traces using conductive epoxy, or wave soldering.

FIG. **13** illustrates that the width of the capacitive device may be wider than the width of the conductive traces **86** formed on the circuit board **80**. In this event, the external conductive plates **72** and **74** may be formed with a width that matches that of the traces **86**, to avoid unintended capacitive coupling to ground plane **84** from plates **72** and **74**. As seen in FIG. **13**, when plates **72** and **74** (plate **72** being seen in FIG. **13**) are the same width as the traces **86**, no additional capacitive coupling to ground is created by plates **72** and **74**. The width of the internal plates such as **66**, **68**, **76**, **10** and **11** may be made narrow as well, but likely can be made as wide as the entire device, for the reason that plates **72** and **74** are substantially closer to ground plane **84** than the other plates internal to the device and thus are more likely to create coupling to ground.

FIGS. **14** and **15**A illustrate a further embodiment of a capacitor **120** comprised of an integrated capacitor array. Overlapping conductive plates **10**, **11** are connected to external conductive contacts **12**, **13**, respectively. Conductive pads **121**, **122** extend over respective upper and lower surfaces of the capacitor **120** and are electrically connected to the contact **12**. Similarly, conductive pads **123**, **124** also extend over respective upper and lower surfaces of the capacitor **120** are connected to the contact **13**. The conductive pads **121**–**124** facilitate mounting the capacitor **120** to circuits on a printed circuit board. As previously described, a lower frequency, higher value capacitor section **60** provides a plurality of parallel capacitances **75** between conductive plates **10**, **11**.

The ends **125**, **126** of the respective conductive pads **121**, **123** are disposed on the upper surface of the capacitor **120** sufficiently close to each other so that a fringe-effect capacitance **127** (FIG. **15**B) is formed therebetween. The fringe-effect capacitor **127** formed between the ends **125**, **126**, of respective pads **121**, **123** provides an integrated, higher frequency, lower value capacitance section **62***a*. In a similar manner, a fringe-effect capacitance **129** is formed between the ends **130**, **131** of the respective pads **122**, **124** on a lower side of the integrated capacitor **120**. The fringe-effect capacitance **129** provides a second, higher frequency, lower value capacitance section **62***b* that is substantially identical to the capacitance section **62***a*. While the fringe effect capacitances **127**, **129** may be relatively small compared to other overlapping parallel plate capacitances **75** within the capacitor **120**, the fringe effect capacitances **127**, **129** have been found to effect the high frequency performance of the capacitor **120**.

The ends **130**, **131** may be separated by only 0.002 of an inch. In order to minimize the opportunity for conduction between the ends **130**, **131** of the respective pads **122**, **124**, an insulating coating or material **132** is provided therebetween. The insulating coating **132** consists of either a high temperature fired insulator, for example, glass, or a low temperature curing material, for example, epoxy, silicone, polymer, etc. However, in other embodiments, depending on the size of the gap between the ends **125**, **126** of respective plates **121**, **123** and other factors, a capacitor designer may choose not to use an insulating material between the ends **125**, **126**. FIG. **14** also illustrates another alternative embodiment in that the ends of the chip are provided with an insulating coating **128** to provide an electrical barrier from shorting with other devices. The insulating coating **128** is substantially similar to the insulating coating **132**. An oxidation process or an anodizing process of the underlying termination material is also compatible and a viable alternative.

FIG. **16** illustrates another example of a broadband capacitor **87** having integrated capacitor array. As shown in FIG. **17**A, the broadband capacitor **87** includes a low frequency, higher value bulk capacitor section **60** comprised of a first plurality of conductive plates **10** connected to an external contact **12** and a second plurality of opposed parallel plates **11** connected to the external contact **13**. As shown in FIG. **17**B, the plates **10**, **11** form capacitors **88** within a bulk capacitance section **60**. It should be noted that the plates **10**, **11** are disposed at an orientation that is substantially perpendicular to a longitudinal centerline **89** of the broadband capacitor **87**. Further, in use, one of the metallized contact areas **12**, **13** is attached to a conductor extending over a major planar surface of a printed circuit board. Thus, the plates **10**, **11** are also substantially perpendicular to the major planar surface of the printed circuit board.

The broadband capacitor **87** further has a pair of higher frequency, lower value capacitor sections **62***a*, **62***b* that are disposed at opposite ends of the bulk capacitor section **60**. Each of the capacitor sections **62***a*, **62***b* has a respective conductive floating plate **90***a*, **90***b* that is not connected to either of the metallized contact areas **12**, **13**. First electrode plates **91***a*, **91***b* form respective capacitors **92***a*, **92***b* with respective floating plates **90***a*, **90***b*. Similarly, electrode plates **93***a*, **93***b* form respective capacitors **94***a*, **94***b* with the respective floating plates **90***a*, **90***b*. The plates **91**, **93** are non-overlapping with each other and operative to provide a series circuit of the capacitors **92**, **94**. In addition, capacitors **95***a*, **95***b* are formed between one of the plates **10** and a respective plate **93***a*, **93***b*.

Referring to FIGS. **18**A and **18**B, another example of an integrated capacitor array is represented by the broadband capacitor **96**. The low frequency capacitance section **60** and high frequency capacitance section **62***b* of FIGS. **18**A and **18**B are substantially identical in construction to the low frequency capacitor section **60** and high frequency capacitor section **62***b* previously described with respect to FIGS. **17**A, **17**B. However, as shown in FIG. **18**A, the metallized plates **12**, **13** extend over an end of the capacitor **96** and have respective ends **97**, **98** sufficiently close to each other so as to form a fringe-effect capacitance **99** therebetween as shown in FIG. **18**B. To prevent conduction between the plate ends **97**, **98**, the space therebetween is filled with an insulating material **132** as described with respect to FIGS. **14** and **15**; however, as will be appreciated, the use of such a coating is optional and depends on many factors.

Referring to FIGS. **19**A and **19**B, a further example of an integrated capacitor array is represented by the broadband capacitor **100**. The low frequency capacitance section **60** is substantially the same as in other embodiments; however, there are differences in the high frequency capacitance sections **62***a*, **62***b*. In high frequency section **62***a*, a pair of conductive electrodes **101**, **102** are disposed between an electrode **11** in the low frequency capacitance section **60** and a first floating electrode **104**. That arrangement of electrodes is effective to provide capacitors **105**, **106**, **107** as shown in FIG. **19**B. Further, as shown in FIG. **19**A, the metallized plates **12**, **13** extend over one end of the broadband capacitor **100** and have respective ends **108**, **109** sufficiently close to each other so as to form a fringe-effect capacitance **110** therebetween as shown in FIG. **19**B. To prevent conduction between the plate ends **108**, **109**, the space therebetween is filled with an insulating material **128** as described with respect to FIGS. **14** and **15**.

In contrast, in the high frequency capacitance section **62***b*, a floating electrode **111** is disposed between a pair of electrodes **112**, **113** and an electrode **10** in the low frequency capacitance section **60**. That arrangement of plates **111**, **112**, **113** with the plate **10** provides capacitors **114**, **115**, **116** as shown in FIG. **20**B. Further, as shown in FIG. **19**A, the metallized plates **12**, **13** also extend over an opposite end of the capacitor **100** and have respective ends **117**, **118** sufficiently close to each other so as to form a fringe-effect capacitance **119** therebetween as shown in FIG. **19**B. However, in contrast to the capacitance section **62***a*, the capacitor design is such that an insulating coating is not required between the plate ends **117**, **118**. In addition, the ends **108**, **109** of respective contact plates **12**, **13** form respective capacitors **135**, **136** with the floating plate **104**.

FIGS. **20**A, **20**B illustrate a still further embodiment of an integrated capacitor array forming a broadband capacitor **133**. FIGS. **20**A, **20**B illustrate an integrated capacitor array that is substantially identical to the previously described capacitor illustrated in FIGS. **10**A, **10**B with two exceptions. First, the floating electrode plate **76** present in FIG. **10**A has been eliminated from the embodiment of FIG. **20**A. Second, the metallized plates **72**, **74** extending from the respective contacts **13**, **12** form a fringe-effect capacitance **79** therebetween. Although small, the fringe-effect capacitance **79** is sufficiently effective at higher frequencies to allow the elimination of the floating plate **76** of FIG. **10**A, thereby reducing the manufacturing cost of the broadband capacitor **133** with respect to the capacitor shown in FIG. **10**A. As will be appreciated, in another embodiment, a capacitor designer may choose to minimize the potential for conduction between ends of the plates **72**, **74** by applying an insulating material in the gap between the plates **72**, **74** similar to the material **132** of FIG. **14**.

In accordance with the foregoing, an improved capacitive device is formed by integrating low and high frequency performance in a single device. Providing one or more higher frequency, lower value capacitors results in fewer resonances and lower insertion loss amplitudes. With less insertion loss, an improved response can be obtained over a substantial bandwidth, for example, 400 KHz–100 GHz. Further, for a particular application, by building and testing capacitive devices using different combinations of the capacitive arrays described herein, a particular size capacitor can be designed to operate over a desired bandwidth.

While the present invention has been illustrated by a description of various embodiments and while these embodiments have been described in considerable detail, it is not the intention of the applicants to restrict or in any way limit the scope of the appended claims to such detail. Additional advantages and modifications will readily appear to those skilled in the art. Specifically, techniques described in these multiple embodiments may be combined in many ways beyond the particular combinations shown herein. For example, the independently adjustable parameters in forming a device in accordance with aspects of the invention include at least the following:

1. the use or not of interior plates **66** and **68** in higher frequency sections **62**,
2. the gap between plates **72** and **74**, **66** and **68**, **97** and **98**, **108** and **109**, **117** and **118**, **125** and **126**, **103** and **131** and the fringe capacitances created thereby,
3. the number of floating plates **76**, **90**, **104**, **111** and their distances from other plates in respective higher frequency sections **62** and adjacent plates in respective lower frequency sections **60**,
4. the width, spacing and overlap characteristics of the floating plates **76**, **90**, **104**, **111**,
5. the extent to which coupling is permitted between non-floating plates in higher frequency sections **62** and adjacent plates in respective lower frequency sections **60**,
6. the use of fringe or face-to-face coupling between floating plates **76**, **90**, **104**, **111** and other plates in respective higher frequency sections **60**,
7. the use of dual or single plates, withdrawn or fully overlapping plates in lower frequency sections **60**, and
8. the relative geometry of external plates **72** and **74** on the device, and the traces **86** on the circuit board to which the device is mounted.

A further potential variable to adjust, is the type of ceramic used. Indeed, different layers in the ceramic structure may be made of ceramic materials having different molecular structures. Different ceramic materials may exhibit different performance in various attributes, such as relative dielectric constant, polarization, breakdown field strength, curing behavior, mechanical strength and mechanical stress and strain behavior. For example, a relatively low dielectric ceramic having relatively good high frequency behavior may be used in the lower section **62** of a device, while a relatively high dielectric ceramic having relatively poorer high frequency behavior may be used in the upper section **60** of the device.

The invention in its broader aspects is therefore not limited to the specific details, representative apparatus and method, and illustrative example shown and described. Accordingly, departures may be made from such details without departing from the spirit or scope of applicant's general inventive concept.

What is claimed is:

1. A capacitor comprising:

a substantially monolithic dielectric body;

a conductive first plate disposed within the dielectric body;

a conductive second plate disposed within the dielectric body and forming a capacitor with the first plate;

a conductive first contact disposed externally on the dielectric body and electrically connected to the first plate; and a conductive second contact disposed externally on the dielectric body and electrically connected to the second plate, and the second contact being located sufficiently close to the first contact to form a first fringe-effect capacitance with the first contact.

2. The capacitor of claim **1** further comprising an insulating layer disposed between the first contact and the second contact on the dielectric body and inhibiting electrical conduction between the first and second contacts.

3. The capacitor of claim **1** wherein the first fringe-effect capacitance is disposed on a first side of the dielectric body and the first contact and the second contact are further disposed on a second side of the dielectric body, and the second contact being located sufficiently close to the first contact on the second side of the dielectric body to form a second fringe-effect capacitance with the first contact.

4. The capacitor of claim **3** further comprising:

a first insulating layer disposed between the first contact and the second contact on the first side of the dielectric body and inhibiting electrical conduction between the first and second contacts; and

a second insulating layer disposed between the first contact and the second contact on the second side of the dielectric body and inhibiting electrical conduction between the first contact and second contact.

5. The capacitor of claim **3** wherein the first side of the dielectric body and the second side of the dielectric body are substantially parallel.

6. The capacitor of claim **1** further comprising conductive first structure disposed within the dielectric body and forming a first capacitor with one of the first and second contacts.

7. The capacitor of claim **6** wherein the conductive first structure forms first and second capacitors with the first and second contacts, respectively.

8. The capacitor of claim **6** wherein the conductive first structure forms a second capacitor with one of the first and second plates.

9. The capacitor of claim **8** wherein the conductive first structure is electrically connected to an other of the first and second plates.

10. The capacitor of claim **1** further comprising:

a conductive first structure disposed within the dielectric body and electrically connected to the first contact, the first structure forming a first capacitor with the first plate; and

a conductive second structure disposed within the dielectric body and electrically connected to the second contact, the second structure forming a second capacitor with the first plate.

11. The capacitor of claim **10** wherein the first structure forms a fringe-effect capacitance with the second structure.

12. The capacitor of claim **11** further comprising a first via of conductive material extending between the first contact and the first structure.

13. The capacitor of claim **12** further comprising a second via of conductive material extending between the second contact and the second structure.

14. The capacitor of claim **13** further comprising a conductive third plate disposed within the dielectric body between the first plate and the first structure and not electrically connected to either the first contact or the second contact, the third plate forming a first capacitor with the first plate and a second capacitor with the first structure.

15. The capacitor of claim **14** wherein the third plate is disposed within the dielectric body between the first plate and the second structure, the third plate forming a third capacitor with the second structure.

16. The capacitor of claim **1** wherein the dielectric body is ceramic.

17. The capacitor of claim **1** wherein the dielectric body comprises ceramic layers of different molecular structure exhibiting different performance in one or more of relative dielectric constant, breakdown field strength, curing behavior, mechanical strength and mechanical stress and strain behavior.

18. The capacitor of claim **1** wherein the ceramic body comprises a plurality of ceramic tape layers laminated together in a green ceramic state and fired to form a cured monolithic ceramic structure.

19. The capacitor of claim **1** wherein the dielectric body has a hexahedron shape, the first and second external conductive contacts being positioned on opposed end surfaces of the hexahedron shape.

20. The capacitor of claim **1** wherein the third conductive plate is substantially smaller in at least one dimension of its planar surfaces, than the first and second conductive plates.

21. A capacitor comprising:

a substantially monolithic dielectric body;

a conductive first and second plates disposed within the dielectric body and forming a capacitor therebetween;

conductive first and second contacts disposed externally on the dielectric body and electrically connected to the first and second plates, respectively; and

a conductive third plate disposed externally on the dielectric body and not electrically connected to either of the first and second contacts, the third plate being located sufficiently close to the first and second contacts to form first and second fringe-effect capacitances with the first and second contacts, respectively.

22. The capacitor of claim **21** wherein the first and second fringe-effect capacitances are serially connected between the first and second contacts.

23. The capacitor of claim **21** further comprising conductive first structure disposed within the dielectric body and forming a first capacitor with one of the first, second and third contacts.

24. The capacitor of claim **23** wherein the conductive first structure forms a second capacitor with one of the first and second plates.

25. The capacitor of claim **24** wherein the conductive first structure is electrically connected to an other of the first and second plates.

26. The capacitor of claim **21** further comprising conductive first structure disposed within the dielectric body and forming first and second capacitors with two of the first, second and third contacts.

27. The capacitor of claim **21** further comprising conductive first structure disposed within the dielectric body and forming first, second and third capacitors with the first, second and third contacts, respectively.

28. A capacitor comprising:

a substantially monolithic dielectric body having a first external surface adapted to be positioned substantially parallel to a major surface of a circuit board; and

a lower frequency, higher value, first capacitor formed by a first plurality of conductive plates disposed within the dielectric body and having respective major surfaces oriented substantially perpendicular to the first external surface, the first plurality of conductive plates forming a plurality of capacitors connected in parallel with each other; and

a higher frequency, lower value, second capacitor formed by a second plurality of conductive plates disposed within the dielectric body and having respective major surfaces oriented substantially perpendicular to the first external surface, the second plurality of conductive plates forming the second capacitor connected in parallel with the first capacitor.

29. The capacitor of claim **28** further comprising a higher frequency, lower value, third capacitor formed by a third plurality of conductive plates disposed within the dielectric body and having respective major surfaces oriented substantially perpendicular to the first external surface, the third plurality of conductive plates forming the third capacitor connected in parallel with the first capacitor and the second capacitor.

30. A capacitor comprising:

a substantially monolithic dielectric body having a longitudinal centerline adapted to extend in a direction substantially parallel to a major surface of a circuit board;

first conductive plates disposed within the dielectric body and having respective major surfaces oriented substantially perpendicular to the longitudinal centerline, the first conductive plates forming at least one lower frequency, higher valued, multilayer capacitor; and

second conductive plates disposed within the dielectric body and having respective major surfaces oriented substantially perpendicular to the longitudinal centerline, the second conductive plates forming at least one higher frequency, lower valued, single layer capacitor.

31. The capacitor of claim **30** wherein the multilayer capacitor and the single layer capacitor are connected in parallel with each other.

32. A capacitor comprising:

a substantially monolithic dielectric body having a first external surface adapted to be positioned substantially parallel to a major surface of a circuit board;

a conductive first plate disposed within the dielectric body at an orientation substantially perpendicular to the first external surface;

a conductive second plate disposed within the dielectric body at an orientation substantially perpendicular to the first external surface and forming a capacitor with the first plate;

a conductive first contact disposed externally on the dielectric body and electrically connected to the first plate;

a conductive second contact disposed externally on the dielectric body and electrically connected to the second plate;

a conductive third plate disposed within the dielectric body at an orientation substantially perpendicular to the first external surface, the third plate not being connected to either the first contact or the second contact, the third plate being located in the dielectric body to form a first capacitor with one of the first plate and the second plate; and

a conductive fourth plate disposed within the dielectric body at an orientation substantially perpendicular to the first external surface, the fourth plate being connected to one of the first contact and the second contact and forming a second capacitor with the third plate.

33. The capacitor of claim **32** wherein the first capacitor is a lower frequency, higher valued capacitor.

34. The capacitor of claim **32** wherein the second capacitor is a higher frequency, lowered valued capacitor.

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